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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/755,740	01/12/2004	Emmanuil H. Lingunis	H1985	1124

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ESCHWEILER & ASSOCIATES, LLC
NATIONAL CITY BANK BUILDING
629 EUCLID AVE., SUITE 1210
CLEVELAND, OH 44114

EXAMINER	
DANG, PHUC T	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/755,740	LINGUNIS ET AL.	
	Examiner	Art Unit	
	PHUC T. DANG	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3,13-15,19 and 20* is/are allowed.

6)☒ Claim(s) *1-12,16-18 and 21-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *073004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on January 12, 2004 is acceptable.

Information Disclosure Statement

2. The office acknowledges receipt of the following items from the applicant:

Information Disclosure Statement (IDS) filed on January 12, 2004 and July 30, 2004.

Specification

3. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 4-10, 12, 16 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al., hereinafter "Yang" (U.S. Patent No. 6,436,768 A1) in view of Chen (U.S. Publication No. US2002/0182829 A1).

Regarding claims 1, Yang discloses a method of forming at least a portion of a SONOS dual bit memory core array upon a semiconductor substrate, the method comprising:

forming a portion of a charge trapping dielectric layer (16, Fig. 2) over the substrate (12, Fig. 2);

forming a resist (18, Fig. 3) over the portion of the charge trapping dielectric layer (16, Fig. 3);

patterning the resist to form a plurality of resist features (18, Fig. 3) having respective first

spacings therebetween (Fig. 3);

removing the patterned resist (18, Fig. 4);

forming the remainder of the charge trapping dielectric layer (22, Fig. 4) over the portion of the charge trapping dielectric layer (16, Fig. 4);

forming a wordline material over the remainder of the charge trapping dielectric layer; and

patterning the wordline material to form wordlines that overlie the bitlines [col. 7, lines 40-50].

Yang discloses all the features of the claimed invention as discussed above, but does not disclose a step of performing a pocket implant through the first spacings and the portion of the

charge trapping dielectric layer, the pocket implant performed at an angle relative to the semiconductor substrate so as to establish pocket implants within the substrate that extend

at least partially under the resist features; performing a bitline implant through the first spacings and the portion of the charge trapping dielectric layer to establish buried bitlines within the substrate having a width corresponding generally to the first spacing, the

bitlines not covering the portions of the pocket implants that extend under the resist features.

Chen, however, discloses a step of performing a pocket implant through the first spacings and the portion of the charge trapping dielectric layer, the pocket implant performed at an angle relative to the semiconductor substrate so as to establish pocket implants within the substrate that extend at least partially under the resist features; performing a bitline implant through the first spacings and the portion of the charge trapping dielectric layer to establish buried bitlines within the substrate having a width corresponding generally to the first spacing, the bitlines not covering the portions of the pocket implants that extend under the resist features [Figs. 4A-4C and [0023] page 3].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the above teaching of Yang as taught by Chen for a purpose of increasing the density of integration of the semiconductor memory device and decreasing the voltage [see [0004] page 1].

Regarding claim 2, Chen discloses a channel (110, Fig. 1) is defined between two buried

bitlines (120, Fig. 1), the portions of pocket implants extending under the resist features changing doping within select portions of the channel [Fig. 1].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the above teaching of Yang as taught by Chen for a purpose of increasing the density of integration of the semiconductor memory device and decreasing the voltage [see [0004] page 1].

Regarding claim 4, yang discloses forming a portion of a charge trapping dielectric layer comprises: forming a first insulating layer (14, Fig. 2) over the semiconductor substrate (12, Fig. 2); and forming a charge trapping layer (16, Fig. 2) over the first insulating layer (14, Fig. 2).

Regarding claim 5, Yang discloses a step of forming the remainder of the charge trapping dielectric layer comprises: forming a second insulating layer (22, fig. 3) over the charge trapping layer (16, fig. 3).

Regarding claim 6, Yang discloses the first and second insulating layers comprise at least one of one or more silicon-rich silicon dioxide layers, one or more oxygen-rich silicon dioxide layers, one or more thermally grown or deposited oxide layers, materials having a high dielectric constant and one or more nitrided oxide layers [col. 6, lines 8-14].

Regarding claim 7, Yang discloses the charge trapping layer comprises at least one of one or more silicon-rich silicon nitride layers and one or more nitrogen-rich silicon nitride layers [col. 6, lines 5-7].

Regarding claims 8-10, Yang discloses the thickness of the first and second insulating layers and the charge trapping layer applied in the process [col. 6, lines 14-30].

Regarding claim 12, Chen discloses the pocket implant includes boron [[0024] page 3].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the above teaching of Yang as taught by Chen to improve the process.

Regarding claim 16, Yang discloses the wordlines are oriented at substantially right angles relative to the buried bitlines [col. 7, lines 40-48].

Regarding claim 27, Yang discloses at least a portion of a SONOS dual bit memory core array formed upon a semiconductor substrate comprising:

a first insulating layer (14, fig. 2) that is not patterned, and is formed over the substrate 912, fig. 2);

a charge trapping layer (16, fig. 2) that is not patterned, and is formed over the first insulating layer (14, fig. 2);

a second insulating layer (22, Fig. 4) that is not patterned, and is formed over the charge

trapping layer (16, Fig. 4);

a pair of bitlines (20, fig. 4) buried within the substrate (12, fig. 4) and defining a channel there-between (Fig. 4).

Yang discloses all the features of the claimed invention as discussed above, but does not disclose pocket implants implanted into the substrate, the bitlines covering some of the pocket implants and some of the pocket implants extending into the channel, the portions

of the pocket implants extending into the channel changing doping within select portions of the channel.

Chen, however, discloses pocket implants implanted into the substrate, the bitlines covering some of the pocket implants and some of the pocket implants extending into the channel, the portions of the pocket implants extending into the channel changing doping within select portions of the channel [Figs. 4A-4C and [0023]].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the above teaching of Yang as taught by Chen for a purpose of increasing the density of integration of the semiconductor memory device and decreasing the voltage [see [0004] page 1].

5. Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (U.S. Publication No. US/2002/0182829 A1) in view of Yang et al., hereinafter "Yang" (U.S. Patent No. 6,436,768 A1).

Regarding claim 21, Chen discloses a method of forming at least a portion of a SONOS dual bit memory core array upon a semiconductor substrate, the method comprising:

forming pocket implants (360, Fig. 3B) within the substrate without patterning a first insulating layer (310, Fig. 3B) overlying the substrate or a charge trapping layer overlying the first insulating layer, the pocket implants being implanted at least partially under features formed out a resist material overlying the charge trapping layer and through the first insulating layer, the

charge trapping layer and first spacings formed between the resist features (420, Figs. 4A-4B);

forming bitline implants (460, Fig. 4C) through the first spacings to establish buried bitlines within the substrate (400, Fig. 4C) having respective widths corresponding generally to the first spacings, the bitlines not covering the portions of the pocket implants that extend under

the resist features.

Chen discloses all the features of the claimed invention as discussed above, but does not disclose the steps of removing the resist features; forming a second insulating layer over the charge trapping layer; forming a wordline material over the second insulating layer; and

patterning the wordline material to form wordlines that overlie the bitlines.

Yang, however, discloses the steps of removing the resist features (18, Fig. 4); forming a second insulating layer (22, Fig. 4) over the charge trapping layer (16, Fig. 4); forming a wordline material over the second insulating layer; and patterning the wordline material to form wordlines that overlie the bitlines [col. 7, lines 40-50].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the above teaching of Chen as taught by Yang for a purpose of improving scaling and providing the charge trapping layer having uniform and precise thickness.

Regarding claims 22-23, yang discloses the first and second insulating layers comprise at least one of one or more silicon-rich silicon dioxide layers, one or more oxygen-rich silicon dioxide layers, one or more thermally grown or deposited oxide layers and one or more nitrided oxide layers and the charge trapping layer comprises at least one of one or more silicon-rich silicon nitride layers and one or more nitrogen-rich silicon nitride layers [col. 6, lines 5-14].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the above teaching of Chen as taught by Yang for a purpose of improving scaling and providing the charge trapping layer having uniform and precise thickness.

6. Yang and Chen discloses the claimed invention except for the process parameters as claimed in claims 11, 17-18, and 24-26. However, the selection of the claimed process parameters would have been obvious to one having ordinary skill in the art at the time the invention was made to improve the charge trapping dielectric layer in the process, since it is well settle that when the general conditions of a claim are discloses in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Allowable Subject Matter

7. The following is a statement of reason for the indication of allowable subject matter:

Claims 3, 13-15 and 19-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

None of the Prior Art made of record discloses the bitline implant is performed before the pocket implant as cited in claim 3 and the bitline implant includes at least one of arsenic, phosphorous and antimony as cited in claim 13 and performing a threshold adjustment implant into the semiconductor substrate prior to forming the portion of the charge trapping dielectric layer as cited in claim 19.

Claims 14-15 and 20 are directly or indirectly depend on claims 13 and 19, then, they also would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is (571) 272-1776. The examiner can normally be reached on 8:00 am-5:00 pm.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and After Final communications.

10. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Phuc T. Dang PD

Primary Examiner

Art Unit 2818